CLAIMS

1. (original) A programmable device having programmable input/output (I/O) circuitry and programmable logic connected to receive incoming signals from and provide outgoing signals to the I/O circuitry, the programmable device comprising:

a first pad and a second pad; and

a programmable I/O circuit (PIC) associated with the first and second pad, wherein the PIC comprises:

a first output buffer adapted to present a first outgoing signal at the first pad and adapted to present the first outgoing signal at the second pad; and

a first switch connected between the first pad and the first output buffer to selectively present the first outgoing signal at the first pad; and

a second switch connected between the second pad and the first output buffer to selectively present the first outgoing signal at the second pad.

2. (original) The invention of claim 1, wherein:

the first switch is a first transmission gate;

the first transmission gate is adapted to be closed when the first output buffer is selected to present the first outgoing signal at the first pad; and

the first transmission gate is adapted to be open when the first output buffer is selected not to present the first outgoing signal at the first pad, wherein capacitive loading at the first pad due to the first output buffer is lower when the first transmission gate is open than when the first transmission gate is closed.

3. (original) The invention of claim 1, wherein the first and second switches are individually controllable.

4. (original) The invention of claim 1, wherein the first output buffer is a single-ended output buffer.

5. (original) The invention of claim 1, wherein the PIC further comprises:

one or more other output buffers, each adapted to present an other outgoing signal at the first pad and the second pad; and

for each other output buffer:

a first other switch connected between the first pad and the corresponding other output buffer to selectively present the corresponding other outgoing signal at the first pad; and

a second other switch connected between the second pad and the corresponding other output buffer to selectively present the corresponding other outgoing signal at the second pad.

6. (original) The invention of claim 1, wherein:

the device further comprises third and fourth pads associated with the PIC; and

the first output buffer is a double-ended output buffer adapted to present a two-leg output signal at the first and third pads.

7. (original) The invention of claim 6, wherein the double-ended output buffer is a differential output buffer and the two-leg output signal is a differential output signal.

8. (original) The invention of claim 6, wherein the double-ended output buffer is a current-mode logic (CML) output buffer and the two-leg output signal is a CML output signal.

9. (original) The invention of claim 6, wherein the PIC further comprises output leg circuitry connected to the two outputs of the double-ended output buffer and adapted to selectively present the two-leg output signal either at the first and third pads or at the second and fourth pads.

10. (original) The invention of claim 9, wherein the selection of the first and third pads is mutually exclusive of the selection of the second and fourth pads.

11. (original) The invention of claim 9, wherein the first and third pads are associated with a flip-chip configuration, and the second and fourth pads are associated with a wire-bond configuration.

12. (original) The invention of claim 9, wherein the output leg circuitry enables both pairs of pads to share pre-drive and reference circuitry of the double-ended output buffer.

13. (original) The invention of claim 9, wherein the output leg circuitry comprises compensation circuitry to compensate for variations in common-mode voltage between the selected pair of pads.

14. (original) The invention of claim 9, wherein capacitance associated with the first and third pads is shielded from the second and fourth pads, and vice versa.

15. (original) The invention of claim 1, wherein the PIC further comprises:
a first input receiver adapted to receive a first incoming signal from the first pad; and
a second input receiver adapted to receive a second incoming signal from the second pad.

16. (original) The invention of claim 1, wherein the PIC further comprises a first input receiver adapted to selectively receive a first incoming signal from the first pad and a second incoming signal from the second pad.

17. (original) The invention of claim 16, wherein the PIC further comprises one or more muxes connected between the first input receiver and the first and second pads to control the selection of the first and second incoming signals for receipt by the first input receiver.

18. (original) The invention of claim 1, wherein:
the programmable device is an FPGA;
the first switch is a first transmission gate;
the first transmission gate is adapted to be closed when the first output buffer is selected to present the first outgoing signal at the first pad;
the first transmission gate is adapted to be open when the first output buffer is selected not to present the first outgoing signal at the first pad, wherein capacitive loading at the first pad due to the first output buffer is lower when the first transmission gate is open than when the first transmission gate is closed;
the first and second switches are individually controllable;
the first output buffer is a single-ended output buffer;
the device further comprises third and fourth pads associated with the PIC; and
the PIC further comprises:
one or more other output buffers, each adapted to present an other outgoing signal at the first pad and the second pad; and
for each other output buffer:
a first other switch connected between the first pad and the corresponding other output buffer to selectively present the corresponding other outgoing signal at the first pad; and

a second other switch connected between the second pad and the corresponding other output buffer to selectively present the corresponding other outgoing signal at the second pad;

a double-ended output buffer; and

output leg circuitry connected to the two outputs of the double-ended output buffer and adapted to selectively present the two-leg output signal either at the first and third pads or at the second and fourth pads, wherein:

the selection of the first and third pads is mutually exclusive of the selection of the second and fourth pads;

the first and third pads are associated with a flip-chip configuration, and the second and fourth pads are associated with a wire-bond configuration;

the output leg circuitry enables both pairs of pads to share pre-drive and reference circuitry of the double-ended output buffer;

the output leg circuitry comprises compensation circuitry to compensate for variations in common-mode voltage between the selected pair of pads; and

capacitance associated with the first and third pads is shielded from the second and fourth pads, and vice versa.

19. (original) A programmable device having programmable input/output (I/O) circuitry and programmable logic connected to receive incoming signals from and provide outgoing signals to the I/O circuitry, the programmable device comprising:

at least four pads;

a programmable I/O circuit (PIC) associated with the four pads, wherein the PIC comprises:

a first plurality of single-ended output buffers, each adapted to present a single-ended output signal at first and second output pads;

a second plurality of single-ended output buffers, each adapted to present a single-ended output signal at third and fourth output pads; and

at least one double-ended output buffer adapted to present a two-leg output signal at the first and third pads; and

two or more input receivers adapted to receive input signals from the four pads.

20. (original) The invention of claim 19, wherein the double-ended output buffer is a differential output buffer.

21. (original) The invention of claim 19, wherein the double-ended output buffer is a CML output buffer.

22. (original) The invention of claim 19, wherein the double-ended output buffer is further adapted to selectively present the two-leg output signal at the second and fourth pads.

23. (original) The invention of claim 22, wherein the selection of the first and third pads or the second and fourth pads is mutually exclusive.

24. (original) The invention of claim 19, wherein the two or more input receivers comprise four input receivers, each adapted to receive an input signal from a different one of the four pads.

25. (original) The invention of claim 19, wherein:

a first input receiver is adapted to receive input signals from both the first and second pads; and

a second input receiver is adapted to receive input signals from both the third and fourth pads.

26. (original) A programmable device having programmable input/output (I/O) circuitry and programmable logic connected to receive incoming signals from and provide outgoing signals to the I/O circuitry, the programmable device comprising:

at least four pads; and

a double-ended output buffer adapted to selectively present a two-leg outgoing signal at first and third pads and adapted to selectively present the two-leg outgoing signal at second and fourth pads, wherein the selection of the first and third pads or the second and fourth pads is mutually exclusive.

27. (original) The invention of claim 26, wherein the double-ended output buffer is a differential output buffer.

28. (original) The invention of claim 26, wherein the double-ended output buffer is a CML output buffer.

29. (original) The invention of claim 26, wherein the PIC further comprises output leg circuitry connected to the two outputs of the double-ended output buffer and adapted to selectively present the two-leg output signal either at the first and third pads or at the second and fourth pads.

30. (original) The invention of claim 29, wherein the output leg circuitry enables both pairs of pads to share pre-drive and reference circuitry of the double-ended output buffer.

31. (original) The invention of claim 29, wherein the output leg circuitry comprises compensation circuitry to compensate for variations in common-mode voltage between the selected pair of pads.

32. (original) The invention of claim 26, wherein the first and third pads are associated with a flip-chip configuration, and the second and fourth pads are associated with a wire-bond configuration.

33. (original) The invention of claim 26, wherein capacitance associated with the first and third pads is shielded from the second and fourth pads, and vice versa.

34. (currently amended) A programmable device having programmable input/output (I/O) circuitry and programmable logic connected to receive incoming signals from and provide outgoing signals to the I/O circuitry, the programmable device comprising:

a first pad <u>and a second pad</u>; and

a programmable I/O circuit (PIC) associated with the first pad <u>and the second pad</u>, wherein the PIC comprises:

a first output buffer adapted to present a first outgoing signal at the first pad;

a first switch connected between the first pad and the first output buffer to selectively present the first outgoing signal at the first pad;

a second output buffer adapted to present a second outgoing signal at the first pad; and

a second switch connected between the first pad and the second output buffer to selectively present the second outgoing signal at the first pad, <u>wherein at least one of the first and second output buffers is further adapted to present its outgoing signal at the second pad</u>.